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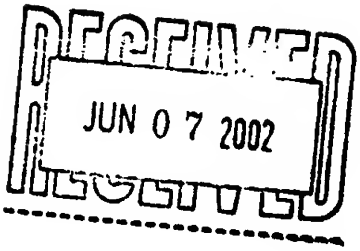
February 22, 2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231



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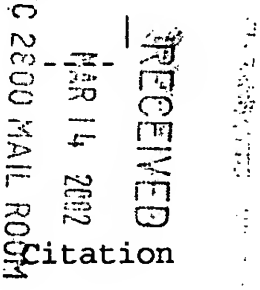
Subject: Serial No. 10/043,605 01/14/02

John Briar

A DISPOSABLE MOLD RUNNER GATE FOR SUBSTRATE BASED ELECTRONIC PACKAGES

Grp. Art Unit: 2822



INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on February 27, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B Ackerman 2/27/02

U.S. Patent 5,635,671 to Freyman et al., "Mold Runner Removal from a Substrate-Based Packaged Electronic Device," describes a degating region having a material formed thereon chosen such that the material in the degating region forms a weak bond with the encapsulant used.

U.S. Patent 5,099,101 to Millerick et al., "Laser Trimming System for Semiconductor Integrated Circuit Chip Packages," describes an automatic laser trimming apparatus for semiconductor integrated chip packages which performs deflashing and degating operations.

U.S. Patent 4,954,308 to Yabe et al., "Resin Encapsulating Method," describes a resin encapsulating method using upper and lower half molds.

U.S. Patent 5,311,402 to Kobayashi et al., "Semiconductor Device Package Having Locating Mechanism for Properly Positioning Semiconductor Device Within Package," describes an integrated circuit chip bonded to a circuit board with a cap for hermetically sealing the chip.

Sincerely,

Stephen B Ackerman

Stephen B. Ackerman,
Reg. No. 37761